



Atacama Large Millimeter Array

Interface Control Document

From: 64 Antenna Correlator
To: Computing Correlator Software

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1 Description

1.1 Purpose

The ALMA correlator processes signals from a total of 64 antennas, in four separate correlator quadrants, one quadrant for each of the four baseband pairs. All four quadrants are controlled and monitored by a single Correlator Control Computer (CCC). Each individual quadrant produces data to be processed by a cluster of four Correlator Data Processing (CDP) computers (16 individual CDP computers total for the four correlator quadrants). There is one additional Master CDP computer.

There is one backup CCC and one backup Master CDP computer. These computers will normally be in a powered down state but physically connected to all necessary interfaces so that they may quickly substitute for the primary computers in response to remote commands.

The Correlator System Racks consist of eight racks in each of four quadrants. In each correlator quadrant the eight system racks consist of four racks identified as Station Racks and four racks identified as Correlator Racks.

1.2 Scope

This ICD covers the electrical interface requirement between the correlator and the CCC and CDP computers. The software/control function interface is included by reference to other documents.

2 Related Documents and Drawings

2.1 References

2.1.1 CAN Protocol Definition Documents

CORL-60.02.03.00-001-A-PLA (Status: Draft)

CAN Protocol Plan:

Correlator Control Computer \leftrightarrow Long Term Accumulator / Correlator Control Card

CORL-60.01.05.00-001-A-PLA (Status: Draft)

CAN Protocol Plan:

Correlator Control Computer \leftrightarrow Station Control Card



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CORL-60.02.05.00-001-A-PLA (Status: Draft)

CAN Protocol Plan:

Correlator Control Computer \leftrightarrow Quadrant Control Card

CORL-60.02.04.00-001-A-PLA (Status: TBD)

CAN Protocol Plan:

Correlator Control Computer \leftrightarrow Final Adder Card

CORL-60.03.02.00-001-A-PLA (Status: TBD)

CAN Protocol Plan:

Correlator Control Computer \leftrightarrow Data Interface Card

2.1.2 Correlator System Manuals

CORL-60.02.03.00-001-A-MAN (Status: Draft)

Long Term Accumulator Sub-System Manual

CORL-60.00.00.00-002-A-MAN (Status: Draft)

C167 Software Projects Manual

2.1.3 Commercial Off The Shelf (COTS) Documentation

User Manual for the PCI64-HPDI32 Card, General Standards Corporation
(www.generalstandards.com)

User Manual for the Infineon C167 Microprocessor (www.infineon.com)



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3 Physical / Electronic Interface Details

There are three categories of physical interfaces:

Category #	Description
1	Direct cable (provided by the correlator IPT) from connector on computer to connector on correlator backplane
2	Cable from connector on computer to a breakout / converter interface box (cable and box provided by the correlator IPT) installed in computer rack
3	Direct cable (provided by the computer IPT) from correlator output data interface (Data Port Interface, installed in computer rack) to computer.

Table 1, Correlator to Computer Physical Interface Categories

There are five signal types between the correlator and computer systems:

Signal Type	Description	Physical Category
CAN Bus	CAN bus between computer and correlator	2
TE	48 msec time event from correlator to computer.	2
RESET	Hardware reset from computer to correlator.	2
Engineering Terminal access	Optional RS-232 access for computer to correlator for bootstrap operations.	1
Correlator Output Data	High data rate parallel output interfaces from correlator to computer.	3

Table 2, Correlator to Computer Signal Types

The signal interfaces consist of four different industry standard electronic signal levels:

- CAN bus logic levels
- RS-232 single ended levels
- TTL single ended levels
- LVDS (Low Voltage Differential Signaling) levels

3.1 Correlator to CCC Interfaces

The CCC and backup CCC computers will be installed in a single computer rack along with a single breakout / converter box. The 2U high breakout box will be installed either above or below the pair of CCC computers (each CCC no more than 4U high) which will be installed in adjacent vertical positions.



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The breakout box (to be designed) provides two simple functions. One function is to breakout multiple signals from internal correlator cables to individual computer connectors. The other is to provide conversion from internal correlator signal levels to TTL levels required by the computers.

3.1.1 CCC CAN Buses

(9 cable assemblies)

The CCC and Backup-CCC computers each have nine CAN buses that connect together in pairs (bus # 0 from each computer form one pair etc.) to control the four correlator quadrants. The following table identifies the nine pairs of CAN buses:

CCC CAN Bus #	Backup CCC CAN Bus #	Breakout Box Connector	Control Correlator System Racks:	
			Quadrant	CAN Bus in
0	0	J1	0	Station Racks
1	1	J2	0	Correlator Racks
2	2	J3	1	Station Racks
3	3	J4	1	Correlator Racks
4	4	J5	2	Station Racks
5	5	J6	2	Correlator Racks
6	6	J7	3	Station Racks
7	7	J8	3	Correlator Racks
8	8	J9	0-3	All 4 Quadrant Control Cards (QCC) on one CAN bus
D-Type 9 pin male	D-Type 9 pin male	D-Type 9 pin male		

Table 3, CCC to Correlator CAN Cables

The correlator IPT will provide the required set of cables for this interface. This set of cables will consist of nine identical cable assemblies. Each cable assembly will daisy chain three D-Type 9 pin female connectors, spaced to fit the three rack mount units. The required 120 ohm / 250 mw line-to-line termination will be installed in the D-Type 9 pin connector shell at the CCC end of the cable furthest from the breakout box. The pinout of each CAN connector is defined in the following table:



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Pin #	Signal	Cable	Terminator
7	CAN-H	Twisted pair, CAT 5 or equivalent	Line-to-line as described above
2	CAN-L		
3	Ground	Ground wire in cable	
1,4,5,6,8,9	NC		

Table 4, CAN Bus Connector Pin Assignments

The CAN Ground line is passed through the breakout box and included in the CAN cables from the breakout box to each quadrant. The CAN buses have 120 ohm, 250 mw, line to line terminations at the last node on the bus in the correlator system racks.

3.1.2 CCC Time Event and RESET Signals (2 cable assemblies)

Correlator Quadrant 0 sources a Time Event signal to the CCC and Backup-CCC computers. The CCC computers use the standard TTL parallel port (e.g. "LPT1") as the input port for the TE signal.

The CCC and Backup-CCC computers source a RESET control signal to each of the four quadrants. The RESET signals provide a hardware reset to the QCC cards. The standard TTL parallel port is also used for these output signals.


CCC LPT Port	Backup CCC LPT Port	Breakout Box Connector
1		J10
	1	J11

Table 5, CCC Parallel Port Cables

The standard parallel port connectors on the CCC computers, and the connectors on the breakout box are D-Type 25 pin female connectors.

The breakout box converts the correlator quadrant 0 TE signal from internal correlator levels to TTL and buffers (fans out) the TTL signals to the two CCC computers.

The RESET signals from the two CCC computers are routed to a logical OR function in the breakout box that automatically responds to RESET signals from which ever CCC computer is active.

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The RESET signals are converted from TTL levels to internal correlator levels in order to drive the correlator quadrants. The breakout box provides pull-up resistors of 4.7K on each RESET input signal.

The pin assignments on these interfaces are shown in the next table:

CORRELATOR SIGNAL NAME	PIN	PC SIGNAL DIRECTION	PC SIGNAL NAME
	1		
RESET-QCC-QUAD0#	2	OUT	DATA0
RESET-QCC-QUAD1#	3	OUT	DATA1
RESET-QCC-QUAD2#	4	OUT	DATA2
RESET-QCC-QUAD3#	5	OUT	DATA3
	6	OUT	DATA4
	7	OUT	DATA5
	8	OUT	DATA6
	9	OUT	DATA7
TE	10	IN	ACK#
	11		
	12		
	13		
	14		
	15		
	16		
	17		
GROUND	18-25		

Table 6, CCC Parallel Port Connector Pin Assignments

The correlator IPT will provide the required set of cables for this interface, consisting of two cables using mating male connectors and flat ribbon cable. The cable lengths will be matched to the spacing of the three rack mount units.

3.1.3 CCC RS-232 Serial Port Signals optional: (8 cable assemblies)

Each correlator quadrant has two multi-drop asynchronous serial port buses used for Engineering terminals. Normally the CCC computer does not require access to these ports. The CCC computer can fully control the correlator via the CAN buses for all operations except a low level bootstrap sequence that may only be performed via these asynchronous serial ports (see Section 7).



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Optional access is provided for CCC to connect to either or both of these buses in order to provide the capability of performing a correlator bootstrap sequence.

One bus serves the Station racks and the second bus serves the Correlator racks (including the Data Port Interface cards). The control of access to these buses is by way of mechanical switches on the QCC cards. Switch SW1 controls the Station bus and SW2 controls the Correlator bus. These switches determine if the correlator ports are connected to the CCC access connectors (defined in the following table) or to the local Engineering terminals.

REF	Description	PCB Conn	Cable Conn (corr end)	Total Number
PF2 (DB9 female)	RS-232 Async Port 1 (Station Racks)	Norcomp 172-009-211-001	TBD	4 (one per quadrant)
PF3 (DB9 female)	RS-232 Async Port 2 (Corr Racks)	Norcomp 172-009-211-001	TBD	4 (one per quadrant)

Table 7, Optional RS-232 Engineering Port Access Cables

In each quadrant, PF2 and PF3 are located in correlator bin C04. Both provide a three wire RS-232 interface. These connectors are configured for straight through wiring to a DTE (Data Terminal Equipment) device. This means CCC appears as a DTE to the correlator, transmitting data into the correlator on pin 3 and receiving data from the correlator on pin 2. The Baud Rate on these interfaces is 57.6K.

Signal Name		REF
	Pin	PF2 and PF3

	1
Data to CCC	2
Data from CCC	3
	4
Ground	5
	6
	7
	8
	9

Table 8, Correlator Engineering Port Connector Pin Assignments



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The correlator IPT will provide the set of cables for this interface if and when it is required. Category 5 LAN type cabling with D-Type 9 pin male connectors on the correlator end will be provided. As indicated, the connector type on the CCC end is TBD.

3.2 Correlator to CDP Data Interfaces (16 commercial cable assemblies)

For each correlator quadrant there are four CDP computers interfaced to four correlator Data Port Interface (DPI) rack mount modules. The four DPI modules are mounted in the same rack as the four CDP computers, each DPI adjacent to the CDP to which it connects.

The CDP end of the data interface uses a commercial High-Speed Parallel Digital Interface that installs in the PCI bus in the CDP computer. This is a PCI64-HPDI32A PCI card from General Standards Corporation. The interface signal levels are LVDS.

The physical cables between the correlator and the CDP computers are from the same commercial source as the PCI cards. The cable is part number CABLE6 SH-PCI64-HPDI32AL-LVDS, a six foot long cable, using Robinson Nugent connectors on each end, part number P50E-080-S-TG (50 mil twisted pair cable). This cable mates with the 80 pin CDP interface connector and with the DPI board mount connectors (Robinson Nugent part number P50E-080-P1-SR1-TG). The cables are provided by the computer IPT.

See the referenced users manual for the PCI64-HPDI32A interface card for the specific pinout of the 80 pin connector. The cable provides a 1 to 1 straight through connection.

3.3 Correlator to Master CDP Physical Interface (2 cable assemblies)

There is only one interface signal between the correlator and the Master CDP computers. This is the TE signal. The interface is identical to the CCC Time Event interface covered in section 3.1.2, consisting of two parallel port cables from the breakout box to the Master CDP and Backup-Master CDP computers. The parallel port DATA0 – DATA7 outputs are not used on this interface.

4 CAN Node Assignments

The CCC commands and monitors the correlator using two CAN buses per quadrant plus one CAN bus for the four Quadrant Control Cards. Each CAN node is an internal peripheral of an Infineon C167 microprocessor.



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4.1 CAN Bus Nodes in Station Racks

One CAN bus per quadrant connects to the 16 Station Control Cards in a set of Station racks. Refer to the referenced CAN Protocol Plan for the Station Control Card for the list of CAN node assignments. The *SET/GET_MY_ANTENNAS* protocol, specifies the set of four antennas associated with CAN nodes 0-15 (decimal) on this bus. These are the only nodes on this bus.

4.2 CAN Bus Nodes in Correlator Racks

The second CAN bus per quadrant connects to targets in the Correlator Racks and to the Data Interface Card nodes (physically located in the CDP racks).

Refer to the referenced CAN Protocol Plan for the Long Term Accumulator (LTA) for the list of CAN node assignments for the LTA nodes (CAN nodes 0-15). These assignments are specified in the *SET/GET_MY_ACCUM_PLANES* and *SET/GET_MY_CONTROL_PLANES* protocols for CAN nodes 0-15 (decimal). The CAN bus in the Correlator racks has six additional nodes:

CAN NODE(dec)	TARGET
16	Final Adder Card A (Final Adders 0 & 3)
17	Final Adder Card B (Final Adders 1 & 2)
24	Data Interface 0
25	Data Interface 1
26	Data Interface 2
27	Data Interface 3

4.3 CAN Bus Nodes for Quadrant Control Cards

One Can bus from the CCC is dedicated to the four QCC cards, one in each quadrant. The CAN node assignments are listed in the following table.

CAN NODE(dec)	TARGET
20	QCC in Quadrant 0
21	QCC in Quadrant 1
22	QCC in Quadrant 2
23	QCC in Quadrant 3



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5 RESET Signal Functional Details

The RESET signals are provided to allow the CCC to reset the QCC C167 microprocessors. The CCC can directly reset the Quadrant Control Card nodes. Reset of either or both of the Station and Correlator rack CAN nodes may be accomplished via CAN protocol commands to be defined in the QCC CAN protocol. All CAN nodes on a bus (either Station or Correlator) are reset globally from the QCC. One possible option is that anytime the QCC is reset as part of the QCC initialization, the QCC will reset both the Station and Correlator buses.

The breakout box in the CCC rack converts the TTL signal from the CCC to internal correlator levels for driving the QCC reset input.

At the TTL output from the CCC parallel port, the RESET signals are low TRUE. If CCC is disconnected or powered down, the pull-ups prevent the QCC from being held reset.

6 TE Signal Functional Details

6.1 Timing Event to CCC and the Master CDP Computers

The TE signals to the CCC and Master CDP parallel ports provides the 48 msec time event signal. The duty cycle is 16 msec HIGH, 32 msec LOW. The positive going transition marks the timing event. The phase of these ticks is independently adjustable to any phase (in 8 nsec increments) with respect to the time event provided to the correlator by the Backend and is synchronous with this signal.

6.2 Timing Event to CDP Computers

The data interface provides a 32 bit, differential LVDS data bus from the correlator to the CDP, along with a clock and seven control / handshake signals (all differential LVDS). One of the seven control signals, GPIO-5, will provide the time event tick to the CDP. GPIO-4 will provide a 16 msec time event for possible use in conjunction with the TE.

The time event signal is a 48 msec event, synchronous to the time event signal provided to the correlator by the Backend. The phase can be adjusted to any 8 nsec position with respect to the TE supplied by the Backend. The duty cycle is 16 msec HIGH, 32 msec LOW. The positive going transition marks the timing event..



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7 Bootstrap Operations (TBD)

Bootstrap operations for the C167 processors on the control cards presently are only controlled by utility software on a PC when a card is first powered up for initial card checkout. This provides low level flash based software in each card that may be used for downloading higher level code for normal operation of the card.

Bootstrap operations controlled by CCC would only be needed to change the low level code in the flash memory used by the C167 processors. This should be so rare as to not require support from the CCC, but the interface provides the capability.

Bootstrap sequences will require either that the CCC utilize the optional RS-232 serial interfaces described in Section 3.1.3 or that boot strap operations only be performed from a PC, independent of CCC.

The CCC would only be able to simultaneously bootstrap every node on either the station bus or the correlator bus. CCC will not have access to the QCC engineering terminal ports.

Bootstrap sequences would require that the CCC command the QCC to perform the hardware level RESET-BOOT steps, after which CCC would use the asynchronous port to perform the bootstrap operations.

See the referenced users manual for the Infineon C167 processor for details of the bootstrap operations. See the referenced C167 Software Projects Manual for additional details of the Minimon utility used when the bootstrap operations are performed from a PC. (CCC would need to implement a functional replacement for the windows based Minimon utility in order to perform the bootstrap operation.)

Updates of the C167 code that is actually run following a RESET operation do not require bootstrap operations.

8 Mechanical Interface

The DPI and Breakout Box modules are standard 19 inch rack mount enclosures, 2U high. This enclosure is manufactured by Hammond, part number RMCV1903BK1. There is one DPI module for each CDP computer, four modules in each CDP rack. There is single Breakout Box module for the CCC computers and one for the Master CDP computers.



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9 Electrical Power Interface

The DPI module contains a built in AC-DC power supply, requiring a universal AC input of 85 - 265 VAC, 47 - 440 Hz. In the initial prototype, a standard 3 prong 115V, 60Hz power cord will be provided with the interface module. The power supply is an Astrodyne Model AS-40-5.

10 Thermal Interface

The data interface module is cooled by an internal fan, operated from the internal 5V power supply. The fan is a Comair-Rotron Model ST05B3

11 Software/Control Function Interface

The control function protocols are defined in the referenced CAN Protocol Plan documents.

12 Safety Interface

The data interface module is subject to the same requirements for fire and earthquake hazard as the correlator as a whole, as specified in ALMA-20.01.02.00-60.00.00.00-A-ICD.